form *pnp* transistors compared with fabricating *npn* transistors. The base width of 50 nm for an *npn* and 30 nm for a *pnp* were achieved simultaneously by low energy ion implantation and rapid thermal annealing for emitter drive in. Cutoff frequencies of 30 and 32, and current gain of 120 and 80 were obtained in *npn* and *pnp* transistors, respectively, in the same chip. Simulated results show that the power dissipation is reduced to 1/5 in a complementary active pull-down circuit compared to the conventional ECL circuit.

It is difficult, however, to achieve same cutoff frequency and the Early voltage because the excess upward diffusion of boron from the buried layer in *pnp* transistor. A lower temperature process is necessary to completely suppress the upward diffusion to obtain the higher Early voltage.

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